

# 74ALVC125-Q100

Quad buffer/line driver; 3-state

Rev. 2 — 20 January 2014

Product data sheet

## 1. General description

---

The 74ALVC125-Q100 is a quad non-inverting buffer/line driver with 3-state outputs. The output enable input ( $\overline{nOE}$ ) controls the 3 state outputs ( $nY$ ). A HIGH on the  $\overline{nOE}$  pin causes the outputs to assume a high-impedance OFF-state.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

## 2. Features and benefits

---

- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
  - ◆ Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Wide supply voltage range from 1.65 V to 3.6 V
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
  - ◆ JESD8-7 (1.65 V to 1.95 V)
  - ◆ JESD8-5 (2.3 V to 2.7 V)
  - ◆ JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ MIL-STD-883, method 3015 exceeds 2000 V
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V ( $C = 200\text{ pF}$ ,  $R = 0\text{ }\Omega$ )



### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ALVC125D-Q100	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74ALVC125PW-Q100	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74ALVC125BQ-Q100	-40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm	SOT762-1

### 4. Functional diagram

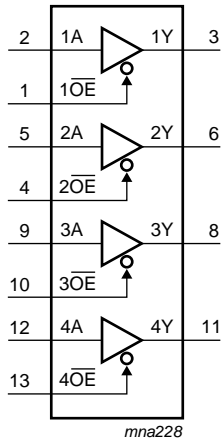


Fig 1. Logic symbol

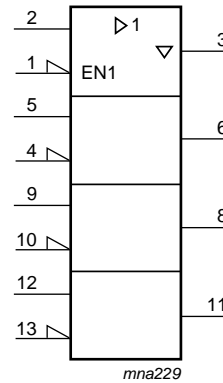


Fig 2. IEC logic symbol

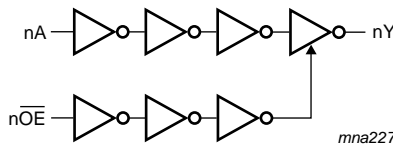
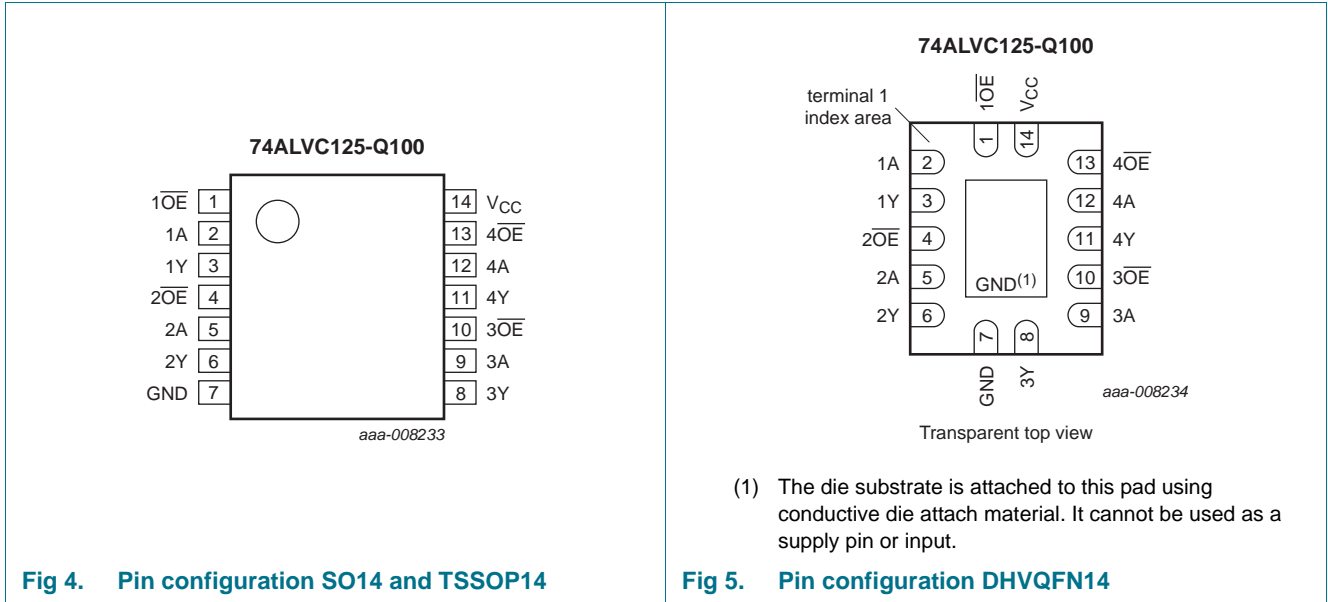


Fig 3. Logic diagram (one buffer)

## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
nA	2, 5, 9, 12	data input
nY	3, 6, 8, 11	bus output
nOE	1, 4, 10, 13	output enable (active LOW)
V <sub>CC</sub>	14	supply voltage
GND	7	ground (0 V)

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Input		Output	
nOE	nA	nY	
L	L	L	
L	H	H	
H	X	Z	

[1] H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 Z = high-impedance OFF-state

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		[1] -0.5	+4.6	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$V_O$	output voltage	output HIGH or LOW state	[1] [2] -0.5	$V_{CC} + 0.5$	V
		output 3-state	-0.5	+4.6	V
		Power-down mode, $V_{CC} = 0$ V	[2] -0.5	+4.6	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +85 °C	[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] When  $V_{CC} = 0$  V (power-down mode), the output voltage can be 3.6 V in normal operation.

[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.

For TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.

For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		1.65	3.6	V
$V_I$	input voltage		0	3.6	V
$V_O$	output voltage	output HIGH or LOW state	0	$V_{CC}$	V
		output 3-state	0	3.6	V
		power-down mode; $V_{CC} = 0$ V	0	3.6	V
$T_{amb}$	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	0	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -100$ $\mu$ A; $V_{CC} = 1.65$ V to 3.6 V	$V_{CC} - 0.2$	-	-	V
		$I_O = -6$ mA; $V_{CC} = 1.65$ V	1.25	1.51	-	V
		$I_O = -12$ mA; $V_{CC} = 2.3$ V	1.8	2.10	-	V
		$I_O = -18$ mA; $V_{CC} = 2.3$ V	1.7	2.01	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	2.2	2.53	-	V
		$I_O = -18$ mA; $V_{CC} = 3.0$ V	2.4	2.76	-	V
		$I_O = -24$ mA; $V_{CC} = 3.0$ V	2.2	2.68	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 100$ $\mu$ A; $V_{CC} = 1.65$ V to 3.6 V	-	-	0.2	V
		$I_O = 6$ mA; $V_{CC} = 1.65$ V	-	0.11	0.3	V
		$I_O = 12$ mA; $V_{CC} = 2.3$ V	-	0.17	0.4	V
		$I_O = 18$ mA; $V_{CC} = 2.3$ V	-	0.25	0.6	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	0.16	0.4	V
		$I_O = 18$ mA; $V_{CC} = 3.0$ V	-	0.23	0.4	V
		$I_O = 24$ mA; $V_{CC} = 3.0$ V	-	0.30	0.55	V
$I_I$	input leakage current	$V_{CC} = 3.6$ V; $V_I = 3.6$ V or GND	-	$\pm 0.1$	$\pm 5$	$\mu$ A

**Table 6. Static characteristics ...continued**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 1.65 V to 3.6 V; V <sub>O</sub> = 3.6 V or GND;	-	±0.1	±10	µA
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	-	±0.1	±10	µA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.2	10	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 3.0 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	5	750	µA
C <sub>I</sub>	input capacitance		-	3.5	-	pF

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit, see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
t <sub>pd</sub>	propagation delay	nA to nY; see <a href="#">Figure 6</a> <sup>[2]</sup>				
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.3	2.4	5.3	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	1.7	3.2	ns
		V <sub>CC</sub> = 2.7 V	-	2.0	3.1	ns
t <sub>en</sub>	enable time	V <sub>CC</sub> = 3.0 V to 3.6 V	1.1	1.8	2.8	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.4	3.9	6.4	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.2	4.1	ns
		V <sub>CC</sub> = 2.7 V	-	2.7	4.3	ns
t <sub>dis</sub>	disable time	V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	1.9	3.5	ns
		n $\overline{O}E$ to nY; see <a href="#">Figure 7</a> <sup>[2]</sup>				
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.8	3.9	5.9	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.1	3.4	ns
		V <sub>CC</sub> = 2.7 V	-	2.9	4.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.4	2.7	4.0	ns

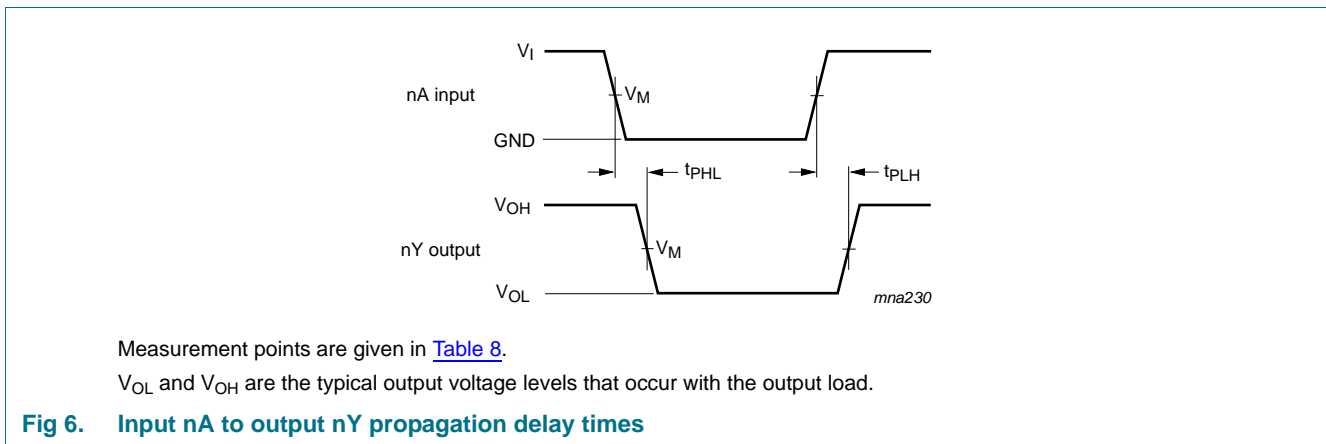
**Table 7. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V). For test circuit, see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
C <sub>PD</sub>	power dissipation capacitance	per buffer; V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 3.3 V <sup>[3]</sup>				
		outputs HIGH or LOW state	-	27	-	pF
		outputs 3-state	-	5	-	pF

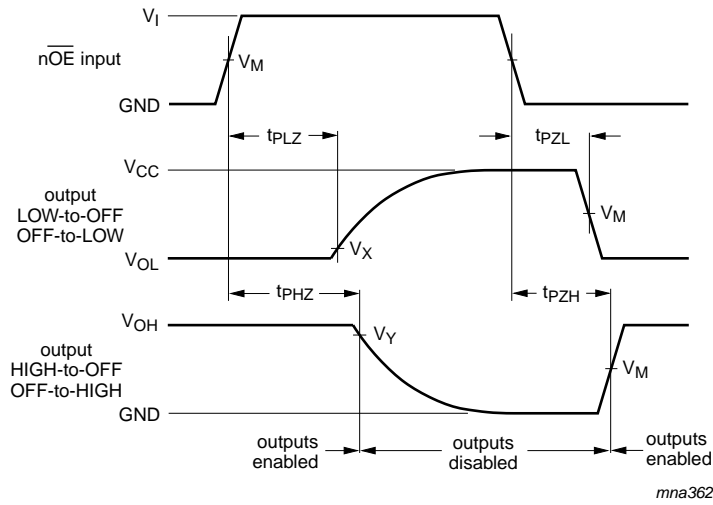
- [1] Typical values are measured at T<sub>amb</sub> = 25 °C
- [2] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.  
t<sub>en</sub> is the same as t<sub>PZH</sub> and t<sub>PZL</sub>.  
t<sub>dis</sub> is the same as t<sub>PHZ</sub> and t<sub>PLZ</sub>.
- [3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> × N + Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) where:  
f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz  
C<sub>L</sub> = output load capacitance in pF  
V<sub>CC</sub> = supply voltage in Volts  
N = number of inputs switching  
Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs

## 11. Waveforms



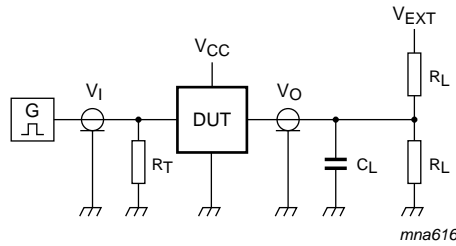
**Table 8. Measurement points**

Supply voltage	Input	Output		
V <sub>CC</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>x</sub>	V <sub>y</sub>
1.65 V to 1.95 V	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V
2.3 V to 2.7 V	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V
2.7 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage levels that occur with the output load.

**Fig 7. Enable and disable times**



Test data is given in [Table 9](#).  
 Definitions for test circuit:  
 $R_L$  = Load resistance.  
 $C_L$  = Load capacitance including jig and probe capacitance.  
 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.  
 $V_{EXT}$  = External voltage for measuring switching times.

**Fig 8. Test circuitry for switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	6 V	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	6 V	GND



12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

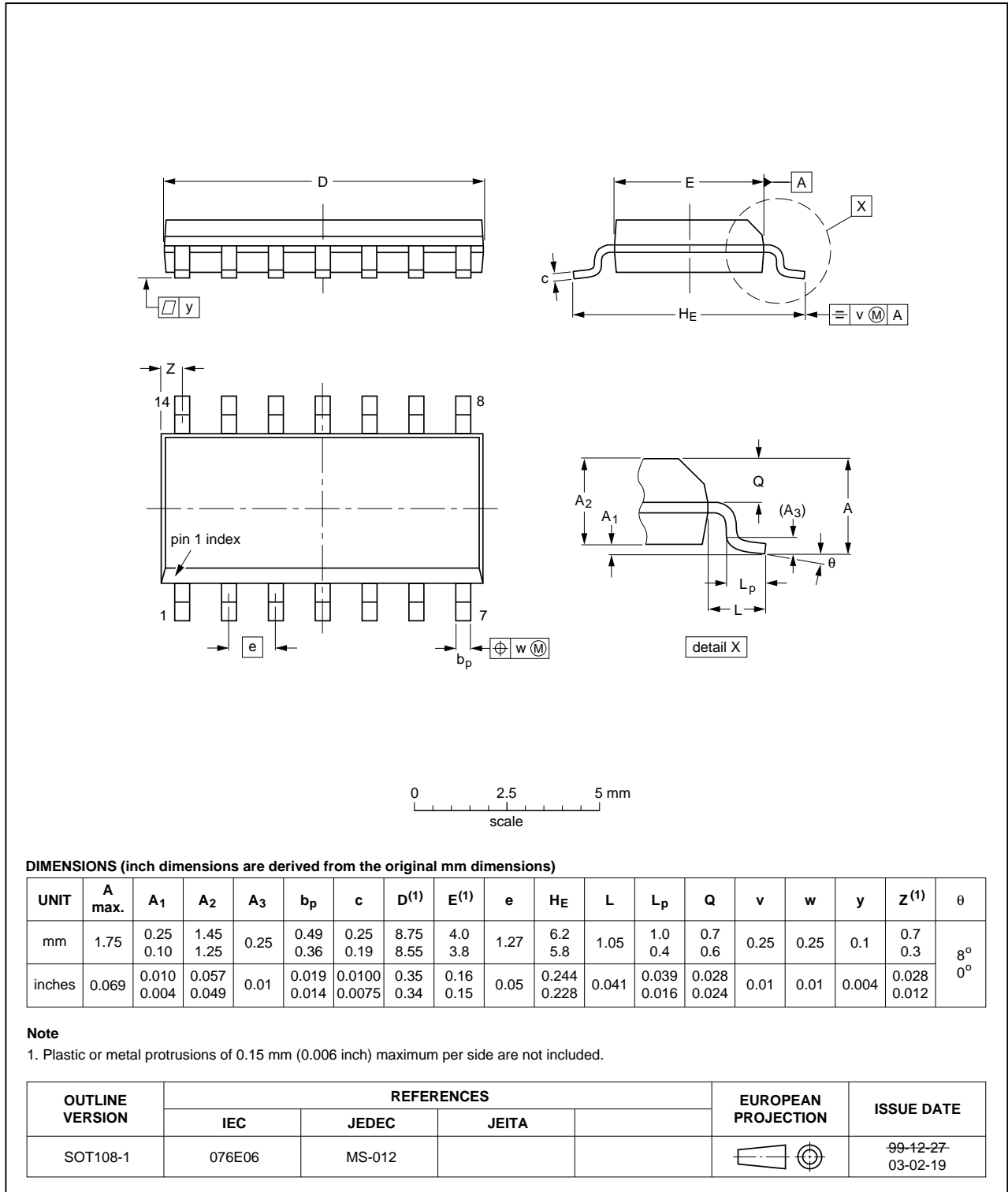


Fig 9. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

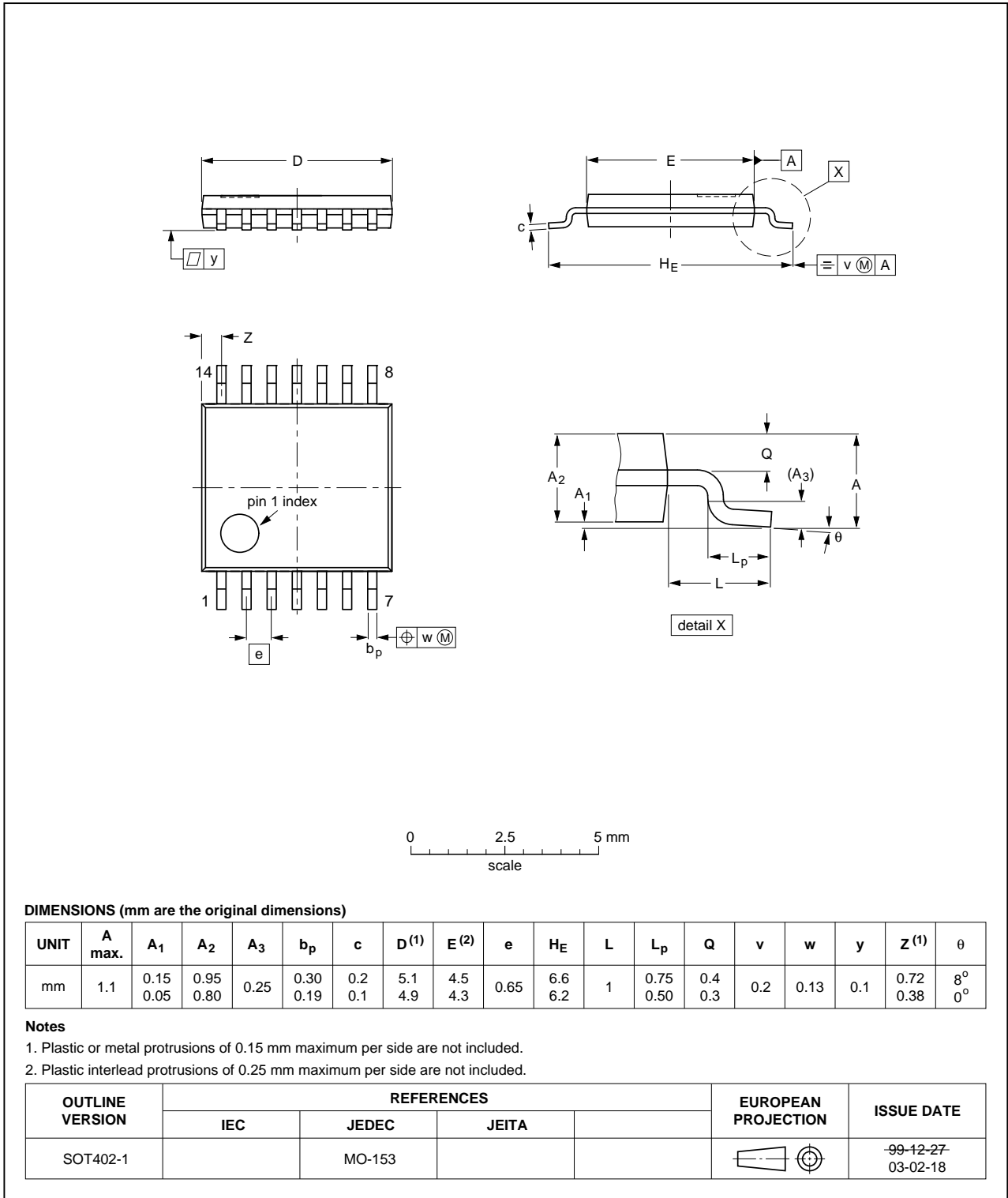


Fig 10. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

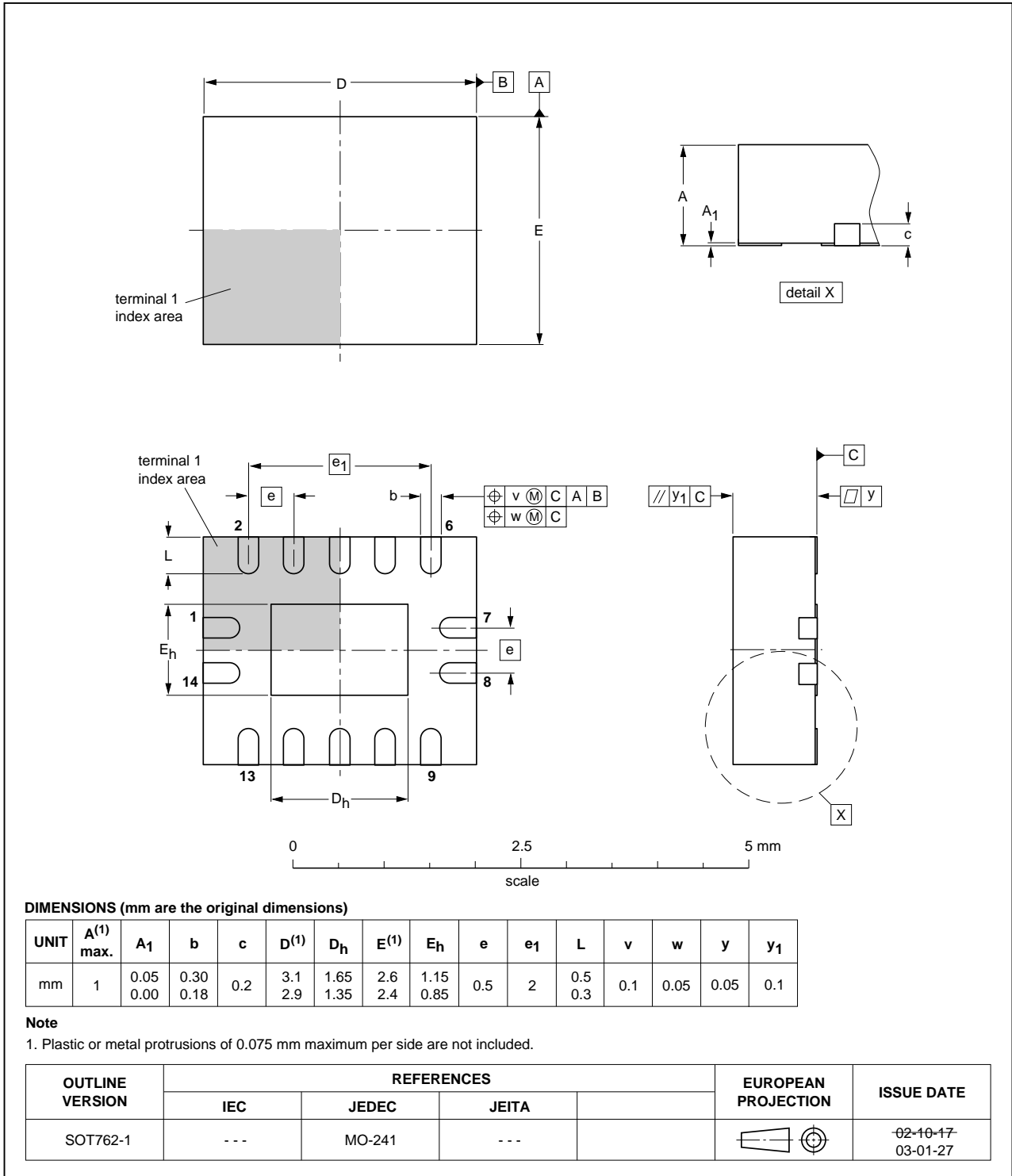


Fig 11. Package outline SOT762-1 (DHVQFN14)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC125_Q100 v.2	20140120	Product data sheet	-	74ALVC125_Q100 v.1
Modifications:	• Feature list corrected (errata).			
74ALVC125_Q100 v.1	20130628	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 15.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 15.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use in automotive applications** — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 16. Contact information

---

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

17. Contents

1 General description . . . . . 1

2 Features and benefits . . . . . 1

3 Ordering information . . . . . 2

4 Functional diagram . . . . . 2

5 Pinning information . . . . . 3

5.1 Pinning . . . . . 3

5.2 Pin description . . . . . 3

6 Functional description . . . . . 3

7 Limiting values . . . . . 4

8 Recommended operating conditions . . . . . 5

9 Static characteristics . . . . . 5

10 Dynamic characteristics . . . . . 6

11 Waveforms . . . . . 7

12 Package outline . . . . . 9

13 Abbreviations . . . . . 12

14 Revision history . . . . . 12

15 Legal information . . . . . 13

15.1 Data sheet status . . . . . 13

15.2 Definitions . . . . . 13

15.3 Disclaimers . . . . . 13

15.4 Trademarks . . . . . 14

16 Contact information . . . . . 14

17 Contents . . . . . 15

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.